UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,875	06/20/2003	Blaine Stackhouse	200207083-1	6673

7590 07/28/2004

EXAMINER
NGUYEN, DANG T

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 07/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,875	STACKHOUSE ET AL.	
	Examiner	Art Unit	
	Dang T Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-20* is/are allowed.

6)☒ Claim(s) *1-3,6,8,9,11 and 21-25* is/are rejected.

7)☒ Claim(s) *4,5,7 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/20/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application and the Information Disclosure Statement filed on June 20, 2003.

2. Claims 1 – 25 are pending in this case. Claims 1, 6, 12, 17, and 21 are independent claims.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 9 recites the limitation wherein "the mode select input" in claim 8. There is insufficient antecedent basis for this limitation in the claim.

No antecedent basis for "the mode select input" provided by claim 8. It is appear to Examiner that claim 7 is providing proper antecedent basis for claim 9.

Claim 11 recites the limitation wherein "the pull-up array transistors" in claim 8. There is insufficient antecedent basis for this limitation in the claim.

No antecedent basis for "the pull-up array transistors" provided by claim 8. It is appear to Examiner that claim 7 is providing proper antecedent basis for claim 11.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Marr U.S. Patent No. 6,496,422 – filed Dec. 8, 2000.

Regarding independent claim 1, Fig. 4 of Marr discloses a bias generator [42] for testing of a static random access memory SRAM [36] comprising: means [45] for adjusting a set of available magnitudes of a bias voltage output signal at an output the bias generator (connection of 44 of 46. See Col. 4 lines 41 – 50) using metal programming (Col. 5 lines 5 – 11).

Regarding dependent claim 2, Fig. 4 of Marr discloses wherein the bias voltage output signal [48] biases a gate of a weak write pull-down transistor [26] of a write driver [WL] in the SRAM [36] with a target magnitude predetermined (Col. 4 lines 47 – 51) for the SRAM [36].

Regarding dependent claim 6, Fig. 5 of Marr discloses a bias generator [42] for testing (Col. 4 lines 44 – 47) of a static random access memory SRAM [36] comprising: a metal programmable transistor [58] that adjusts a set of available magnitudes of a bias voltage output signal at the bias generator output when metal programmed (Col. 5 lines 39 – 50).

5. Claims 1, 3, 6, 8 and 21 - 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Sher et al. U.S. Patent No. 6,756,805 – filed Nov. 15, 2002.

Regarding independent claim 1, Fig. 4 of Sher et al. discloses a bias generator for testing of a static random access memory SRAM (intended of use) comprising: means (Fig. 4 [HIGHVBB1, HIGHVBB2, LOWVBB1, LOWVBB2, NORMVBB]) for adjusting a set of available magnitudes of a bias voltage output signal at an output the bias generator (Col. 9 lines 43 - 58) using metal programming (Fig. 6, Fig. 7).

Regarding dependent claim 3, Sher discloses wherein the means for adjusting comprises a metal-programmable transistor (Fig. 6) in the bias generator, the metal-programmable transistor comprising either or both of a metal-programmable pull-up transistor (Fig. 6 [M17]) and a metal-programmable pull-down transistor (Fig. 6 [RDFUS* transistor]) that change one or both of a range and a resolution of the set of available magnitudes when the metal-programmable transistor is metal programmed (Col. 9 lines 43 - 58).

Regarding independent claim 6, Fig. 4 of Sher discloses a bias generator for testing (Col. 8 lines 47 – 51) of a static random access memory SRAM (intended of use) comprising: a metal programmable transistor (Fig. 6) that adjusts a set of available magnitudes of a bias voltage output signal at the bias generator output when metal programmed (Col. 9 lines 43 - 58).

Regarding dependent claim 8, Sher discloses wherein the metal-programmable transistor comprises either or both of a metal-programmable pull-up transistor (Fig. 6 [RDFUS* transistor]) and a metal-programmable pull-down transistor (Fig. 6 [RDFUS*

transistor]), the metal-programmable transistor changing one or both of a range and a resolution of the set of available magnitudes when metal programmed (Col. 9 lines 43 - 58).

Regarding independent claim 21, Sher et al. discloses a method of modifying a set of available magnitudes of a bias voltage output signal generated by a bias generator comprising (Col. 3 lines 36 – 52): providing a metal-programmable transistor (Fig. 6) in the bias generator (Fig. 4 [HIGHVBB1, HIGHVBB2, LOWVBB1, LOWVBB2, NORMVBB]); and metal programming the metal-programmable transistor (Fig. 6) to connect the transistor to circuitry of the bias generator (Fig. 4), such that a corresponding ON state resistance (Fig. 6 HFS1) of the metal-programmed transistor is combined with an effective ON state resistance (Fig. 7) of the circuitry to modify the available magnitudes of the set (Col. 9 line 43 – Col. 10 line 6).

Regarding dependent claim 22, Sher discloses wherein providing a metal-programmable transistor (Fig. 6) comprises providing either or both of a metal-programmable pull-up transistor (Fig. 6 [RDFUS* transistor]) and a metal-programmable pull-down transistor (Fig. 6 [M17]) in the bias generator, and wherein metal programming the metal-programmable transistor comprises connecting either or both of the metal-programmable pull-up transistor and the metal- programmable pull-down transistor to the bias generator circuitry (Figs. 5 – 7 disclosing internal circuit of bias generator of Fig.4).

Regarding dependent claim 23, Sher discloses wherein metal programming the metal-programmable pull-up transistor (Fig. 6 [RDFUS* transistor]) to connect to the

circuitry combines a corresponding pull-up ON state resistance (Fig. 6 [RDFUS*) of the metal-programmed pull-up transistor (Fig. 6 [RDFUS* transistor]) with an effective ON state resistance (Fig. 6 [HFS]) of a pull-up transistor array, (Fig. 8 [91]) of the bias generator circuitry.

Regarding dependent claim 24, Sher discloses wherein metal programming the metal-programmable pull-down transistor (Fig. 6 [M17]) to connect to the circuitry combines a corresponding pull-down ON state resistance (Fig. 6 [PCA]) of the metal-programmed pull-down transistor (Fig. 6[M17]) with an ON state resistance of a pull-down transistor (Fig. 8 [92]) of the bias generator circuitry.

Regarding dependent claim 25, Sher discloses wherein providing a metal-programmable transistor (Fig. 4) comprises providing either or both of a selection of metal-programmable pull-up transistors (Fig. 8[91]) and a selection of metal-programmable pull-down transistors (Fig. 8 [92]) in the bias generator, at least one of the metal-programmable transistors of each respective selection being different from other metal-programmable transistors of the respective selections, and wherein metal programming the metal-programmable transistor comprises selecting (Fig. 6 [RDFUS*], a respective metal-programmable transistor from either or both the pull-up transistor (Fig. 6 [RDFUS* transistor) selection (Fig. 6 [PCA]) and the pull-down transistor selection (Fig. 6 [M17]), and connecting (Figs. 5 – 7) the selected respective metal-programmable transistor to the bias generator circuitry (Fig. 4).

Allowable Subject Matter

6. Claims 4, 5, 7, and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 9 and 11 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

7. Claims 12 – 20 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 9 and 11 are objected to as being dependent upon a rejected base claim (claim 7 instead of claim 8), but would be allowable if rewritten in appropriation for those claims.

With respect to claim 4, in addition to other elements, the prior arts '422' and '805' as applied above, do not teach a pull-up array of transistors connected between a first supply voltage and the bias generator output; a pull-down transistor connected between the bias generator output and a second supply voltage; and a gate bias circuit connected between a mode select input and a gate of the pull-down transistor, wherein the metal-programmable pull-up transistor is connectable in parallel or in series with the pull-up transistor array, and wherein the metal-programmable pull-down transistor is connectable in parallel or in series with the pull-down transistor.

With respect to claim 7, in addition to other elements, the prior arts '422' and '805' as applied above, do not teach a bias generator having a pull-up array of transistors connected between a first supply voltage and the bias generator output, a pull-down transistor connected between the bias generator output and a second supply voltage; and a gate bias circuit connected between a mode select input and a gate of the pull-down transistor, wherein the metal-programmable transistor is connectable one or both of in series and in parallel with either or both of the pull-up array and the pull-down transistor.

With respect to claims 10, 12 and 17, in addition to other elements in the respective claim, the prior arts '422' and '805' as applied above, do not teach a bias generator having a first transistor having a source connected to drains of the pull-up transistor array, a drain connected to the bias generator output and a gate connected to an inverse mode select input; and a second transistor having a source connected to the second supply voltage, a drain connected to the bias generator output, and a gate connected to the inverse mode select input, wherein the mode select input and the inverse mode select input control a selection between a weak write test mode (WWTM) and a default mode of operation of the bias generator, a set of selection inputs selecting the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic low level at the bias generator output in the default mode.

Prior art

9. *The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.*

Tran et al.	Pub. No.: US 2003/0128594 A1	Pub. Date: Jun. 10, 2003
Chen et al.	Patent No.: US 6,414,889 B1	Date of Patent: Jul. 2, 2002
Weiss et al.	Patent No.: US 6,192,001 B1	Date of Patent: Feb. 20, 2001

Contact Information

10. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (703) 305-1673. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dang Nguyen 7/16/2004

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800